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EXAMINER	
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ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,678	JACOB ET AL.	
	Examiner	Art Unit	
	AIMEE J. LI	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2008 and 24 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 21-25* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 and 21-25 have been considered. Claim1 has been amended as per Applicants' request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: After Final Amendment filed 28 March 2008 and Supplemental After Final Amendment as filed 24 April 2008.

Claim Objections

3. Claim 21 is objected to because of the following informalities: Claim 21 depends on claim 20, but claim 20 has been cancelled. Please correct this to read claim 21 depends on claim 14. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-18 and 21-25 are rejected under 35 U.S.C. 103(a) as being obvious over Kogge, U.S. Patent Number 5,475,856 (herein referred to as Kogge) in view of Free-Online Dictionary of Computing (herein referred to as FOLDOC).

6. Referring to claim 1, Kogge has taught an integrated circuit comprising:

a. a plurality of computational elements (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7,

line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

b. a first and a second processing node each having a core processor with a common architecture, wherein the common architecture is configurable in response to a first configuration command to be a control node adapted to control an interconnection of said computational elements to perform a selected task and configurable in response to a second configuration command to be a programmable scalar node (PSN) adapted to perform a computational application (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

c. a first memory associated with said first processing node (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

d. a second memory associated with said second processing node (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

e. a first interface coupling said core processor of said first processing node to said first memory and to said computational elements (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line

1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

f. a second interface coupling said core processor of said second processing node to said second memory and to said computational elements, the first interface and the second interface having the same architecture (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

7. Kogge has not taught each of said first and second memories including at least one of a data cache and an instruction cache. FOLDOC has taught memories can be caches (FOLDOC search term "cache"). A person of ordinary skill in the art at the time the invention was made would have recognized that a cache is a higher speed memory that increases speed of the processor by not only decreasing the amount of time needed to access memory but also decreasing the need to access slower speed memory. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the caches of FOLDOC in the device of Kogge to increase processor speed.

8. Referring to claim 2, Kogge has taught the integrated circuit of claim 1 further comprising means for temporally adapting said second node and said computational elements to perform a selected function (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

9. Referring to claim 3, Kogge has taught the integrated circuit of claim 2 wherein said temporal means further comprises executable code defining said selected function stored in at least said first memory (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

10. Referring to claim 4, Kogge has not taught the integrated circuit of claim 3 wherein said executable code is downloaded from the Internet by said first processing node. FOLDOC has taught a file is downloaded from the Internet (FOLDOC search term "Internet"). A person of ordinary skill in the art at the time the invention was would have recognized that transferring files, including files holding instructions to be executed by a processor, via the Internet is faster than waiting for the files to be released off system on separate multi-media requiring shipping. Therefore, it would have been obvious to incorporate transferring files via the Internet, as taught by FOLDOC, in the device of Kogge to increase speed of receiving off system files.

11. Referring to claim 5, Kogge has not taught the integrated circuit of claim 4 wherein said executable code comprises operating system code. FOLDOC has taught operating system code (FOLDOC search term "operating system"). A person of ordinary skill in the art at the time the invention was made would have recognized that an operating system controls the operation of the processor, i.e. what tasks are performed when and other control processes. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the operating system of FOLDOC in the device of Kogge to ensure correct operation and control of the processor.

12. Referring to claim 6, Kogge in view of FOLDOC has taught the integrated circuit of claim 5 wherein said first processing node initiates the temporal adaptation of said computational elements and said second processing node to perform said selected function (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

13. Referring to claim 7, Kogge has taught the integrated circuit of claim 1 wherein said plurality of computational elements are adapted to form at least one arithmetic node, at least one of bit-manipulation node and at least one finite state machine nodes (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

14. Referring to claim 8, Kogge has taught the integrated circuit of claim 1 further comprising a plurality of said second processing nodes and an interconnection network, the plurality of said second processing nodes coupled through the interconnection network to said first processing node and plurality of computation elements (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

15. Referring to claim 9, Kogge has taught an integrated circuit comprising:

a. a first node having:

i. a first core processing configurable in response to a first configuration signal to a controller node for execution of code (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23;

column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

ii. a first memory for storing executable code (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

iii. means for transferring executable code and data from said first memory to said first core processor (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

b. a plurality of computational elements adapted to perform a selected function (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

c. a second node having:

i. a second core processor having the same circuit architecture as the first core processor, the second core processor configurable into a RISC processor for execution of application code (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

ii. a second memory for storing application code (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

iii. means for transferring application code and data from said second memory to said second core processor (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

d. an interconnection network coupling said controller node and said RISC processor to said plurality of computational elements to perform the selected function (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

e. a first interface coupling said first core processor to said interconnection network (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

f. a second interface coupling said second core processor to said interconnection network, the first and second interfaces having a common interface architecture (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to

column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

16. Kogge has not taught the executable code is operating system executable code. FOLDOC has taught operating system code (FOLDOC search term "operating system"). A person of ordinary skill in the art at the time the invention was made would have recognized that an operating system controls the operation of the processor, i.e. what tasks are performed when and other control processes. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the operating system of FOLDOC in the device of Kogge to ensure correct operation and control of the processor.

17. Referring to claim 10, Kogge in view of FOLDOC has taught the integrated circuit of claim 9 wherein said first node further comprises a configuration register, said configuration register containing a bit for determining whether said first node functions as the controller node or as a RISC processor (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

18. Referring to claim 11, Kogge in view of FOLDOC has taught the integrated circuit of claim 9 wherein said configuration register bit, when set, protects a portion of memory from access by said computational elements (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

19. Referring to claim 12, Kogge in view of FOLDOC has taught the integrated circuit of claim 9 further comprising a protected portion of memory accessible only to said controller node

(Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

20. Referring to claim 13, Kogge in view of FOLDOC has taught the integrated circuit of claim 9 wherein said first node and said second node further comprise:

a. an interface comprising:

i. a data distributor for receiving an input stream from an external source, said input stream having configuration information, application code or executable code (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

ii. a hardware task manager for receiving configuration information from said data distributor (FOLDOC search term "operating system");

iii. a controller for providing said interface access to a set of registers associated with the corresponding first or second core processor (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

21. Kogge has not taught

i. a DMA engine for receiving data and executable code from said data distributor; and

ii. an interrupt controller for detecting an interrupt condition.

22. FOLDOC has taught a DMA engine (FOLDOC search term "DMA") and interrupts (FOLDOC search term "interrupt"). A person of ordinary skill in the art at the time the invention was made would have recognized that a DMA engine controls access to memory without using CPU resources, thereby freeing up those resources for other tasks and increasing efficiency, and interrupts correct errors, thereby ensuring correction function and execution. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the DMA engine and interrupts of FOLDOC to increase efficiency and ensure correct functionality.

23. Referring to claim 14, Kogge has taught an integrated circuit having a plurality of computational elements and an interconnection network for interconnecting said computational elements, said integrated circuit comprising:

a. a controller node comprising:

i. a first core processor for executing code (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

ii. a first memory for storing executable code (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4); and

iii. a first interface coupled to said first core processor and to the interconnect network for receiving and transferring to the first core processor a portion of an input stream from an external source, said input stream having configuration information or executable code (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4); and

b. a programmable scalar node comprising:

i. a second core processor for executing instructions, the second core processor having the same circuit architecture as the first core processor (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

ii. an instruction memory including an instruction cache for storing said instructions (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4);

iii. a second interface coupled to said second core processor and to the interconnection network for receiving an input stream from the controller node including the instruction memory and the data memory, said input stream having configuration information (Kogge Abstract; column 3, lines

3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

24. Kogge has not taught the code is operating system code and a data memory including an data cache. FOLDOC has taught an operating system and caches (FOLDOC search term "cache"). A person of ordinary skill in the art at the time the invention was made would have recognized that an operating system controls the operation of the processor, i.e. what tasks are performed when and other control processes, and a cache is a higher speed memory that increases speed of the processor by not only decreasing the amount of time needed to access memory but also decreasing the need to access slower speed memory. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the caches of FOLDOC in the device of Kogge to ensure correct operation and control of the processor and to increase processor speed.

25. Referring to claim 15, Kogge has not taught the integrated circuit of claim 14 further comprising means for accessing said first core processor and said first memory to debug error conditions. FOLDOC has taught interrupts as a method for handing error conditions (FOLDOC search term "interrupt"). A person of ordinary skill in the art at the time the invention was made would have recognized that interrupts correct errors, thereby ensuring correction function and execution. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the interrupts of FOLDOC to increase efficiency and ensure correct functionality.

26. Referring to claim 16, Kogge in view of FOLDOC has taught the integrated circuit of claim 14 further comprising means for node-to-node communication (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

27. Referring to claim 17, Kogge in view of FOLDOC has taught the integrated circuit of claim 14 further comprising a second memory for string executable code for controlling the interconnection of said computation elements in response to configuration information (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

28. Referring to claim 18, Kogge in view of FOLDOC has taught the integrated circuit of claim 14 further comprising means for controlling an initiation of operation of said computational element upon reset or power on (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

29. Referring to claim 21, Kogge in view of FOLDOC has taught a memory arbitration unit for managing access to said data memory and said instruction memory (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

30. Referring to claim 22, Kogge in view of FOLDOC has taught the integrated circuit of claim 14 further comprising means for controlling power consumption (FOLDOC search term "operating system").

31. Referring to claim 23, Kogge in view of FOLDOC has taught the integrated circuit of claim 1, wherein the control node is configured to change the interconnecting of said computational elements and said first and second processing nodes to define a second task to achieve a second function previously not available or existent (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

32. Referring to claim 24, Kogge in view of FOLDOC has taught the integrated circuit of claim 1, wherein the PSN node is a RISC processor (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

33. Referring to claim 25, Kogge in view of FOLDOC has taught the integrated circuit of claim 9, wherein the controller node is configured to change the interconnection network coupling said controller node to said computational elements to perform a second selected function previously not available or existent (Kogge Abstract; column 3, lines 3-23 and lines 31-63; column 4, line 29 to column 5, line 23; column 6, line 1 to column 7, line 17; column 8, line 42 to column 9, line 58; Figure 1a; Figure 1b; Figure 3; and Figure 4).

Response to Arguments

34. Applicant's arguments, see After Final Amendment, filed 28 March 2008, and Supplemental After Final Amendment, filed 24 April 2008, with respect to the rejection(s) of claim(s) 1-18 and 21-25 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the rejection above.

Conclusion

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AIMEE J. LI whose telephone number is (571)272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aimee J Li/
Primary Examiner, Art Unit 2183
27 April 2008